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EXAMINER
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LEE, EUGENE

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/762,572  
Filing Date: January 23, 2004  
Appellant(s): TWYNAM, JOHN

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Deborah S. Gladstein  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 11/9/07 appealing from the Office action mailed 1/23/07.

***(1) Real Party in Interest***

A statement identifying by name the real party in interest is contained in the brief.

***(2) Related Appeals and Interferences***

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

***(3) Status of Claims***

The statement of the status of claims contained in the brief is correct.

***(4) Status of Amendments After Final***

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

***(5) Summary of Claimed Subject Matter***

The summary of claimed subject matter contained in the brief is correct.

***(6) Grounds of Rejection to be Reviewed on Appeal***

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The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

***(7) Claims Appendix***

The copy of the appealed claims contained in the Appendix to the brief is correct.

***(8) Evidence Relied Upon***

5,192,987	KHAN	3-1993
6,995,397	YAMASHITA	2-2006
6,639,255	INOUE	10-2003
5,895,929	ABROKWAH	4-1999

***(9) Grounds of Rejection***

The following ground(s) of rejection are applicable to the appealed claims:

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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2. Claims 1, and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. 5,192,987 in view of Yamashita et al. 6,995,397 B2. Khan discloses (see, for example, FIG. 5) a transistor (compound semiconductor FET) comprising a buffer layer (AlN layer) 38, substrate 37; a plurality of III-N layers comprising GaN layer 39 and  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layer 41; source contact (source electrode) 43, gate contact (gate electrode) 47, and drain contact (drain electrode) 44. Khan does not disclose an n-type delta doped GaN layer. However, Yamashita discloses (see, for example, FIG. 1) a semiconductor device comprising a channel layer 20 wherein the channel layer comprises an n-type undoped layer 22, and an n-type delta doped layer 21. In column 23, lines 1-6, Yamashita discloses that GaN may be used. In the abstract, Yamashita discloses the electric field in the surface regions is weakened, thereby allowing the current drive force to increase. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an n-type delta doped GaN layer in order to increase the current drive force of the transistor.

Regarding the limitation "AlN layer" in line 2 of claim 1, see, for example, column 4, lines 19-20 wherein Khan discloses the buffer layer comprising aluminum nitride (AlN).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. '987 in view of Yamashita et al. '397 B2 as applied to claims 1, and 2 above, and further in view of Phillips 6,770,902 B2. Khan in view of Yamashita does not disclose an insulating layer. However, Phillips discloses (see, for example, figure) a transistor comprising a gate insulation layer 32. In column 5, lines 58-65, Phillips discloses that the gate insulation layer forms a MISFET instead of a Schottky contact. Therefore, it would have been obvious to one of ordinary

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skill in the art at the time of invention to have an insulating layer in order to form another semiconductor device such as a MISFET (instead of a Schottky contact).

4. Claims 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. '987 in view of Yamashita et al. '397 B2 as applied to claims 1, and 2 above, and further in view of Inoue 6,639,255 B2. Khan in view of Yamashita does not disclose each of the semiconductor layers being of a C-plane Ga-surface type. However, Inoue discloses (see, for example, abstract) a semiconductor device comprising layers that have c facets of Ga atoms (C-plane Ga-surface type). In column 10, lines 65-67, Inoue discloses that such a structure prevents an increase of the source resistance and reduction of the leakage current. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have each of the semiconductor layers being of a C-plane Ga-surface type in order to prevent an increase of the source resistance and reduce the leakage current.

Regarding lines 5-6 of claim 5, Khan in view of Yamashita does not disclose the sheet doping concentration of the n-type delta doped III-N layer being within a range of  $1 \times 10^{13} \text{ cm}^{-2}$  to  $2 \times 10^{13} \text{ cm}^{-2}$ . However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the sheet doping concentration of a n-type delta doped III-N layer in order to increase the current drive force by weakening the electric field in the surface region. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have sheet doping concentration of the n-type delta doped III-N layer is within a range of  $1 \times 10^{13} \text{ cm}^{-2}$  to  $2 \times 10^{13} \text{ cm}^{-2}$  because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the sheet doping

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concentration in order to increase the current drive force by weakening the electric field in the surface region. See *In re Aller*, 105 USPQ 233.

Regarding lines 5-6 of claim 6, Khan in view of Yamashita does not disclose the sheet doping concentration of the n-type delta doped III-N layer being within a range of  $5 \times 10^{12} \text{ cm}^{-2}$  to  $1.5 \times 10^{13} \text{ cm}^{-2}$ .” However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the sheet doping concentration of a n-type delta doped III-N layer in order to increase the current drive force by weakening the electric field in the surface region. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have sheet doping concentration of the n-type delta doped III-N layer is within a range of  $5 \times 10^{12} \text{ cm}^{-2}$  to  $1.5 \times 10^{13} \text{ cm}^{-2}$  because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the sheet doping concentration in order to increase the current drive force by weakening the electric field in the surface region. See *In re Aller*, 105 USPQ 233.

Regarding the limitation “substrate is sapphire” in line 2 of claim 5, see, for example, column 2, lines 41-43, wherein Khan discloses the material of the substrate being sapphire.

Regarding the limitation “substrate is SiC” in line 2 of claim 6, see, for example, column 6, lines 7-10, wherein Khan discloses the material of the substrate being silicon carbide (SiC).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. ‘987 in view of Yamashita et al. ‘397 B2 as applied to claims 1, and 2 above, and further in view of Abrokwhah et al. 5,895,929. Khan in view of Yamashita does not disclose an electronic circuit provided with the compound semiconductor FET. However, Abrokwhah discloses (see, for

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example, column 1, lines 15-46) FETS being part of electronic circuits such as logic and control circuits, high speed digital circuits, and the like. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an electronic circuit provided with the compound semiconductor FET in order to integrate the transistors in more robust devices.

***(10) Response to Argument***

Regarding the appellant's argument on the bottom of page 4 of the appeal brief filed 11/9/07 that "the dopant concentration in Yamashita's structure is not selected to reduce discontinuity of the electric field at the interface between the AlN layer and the undoped GaN layer", this argument is not persuasive. The fact that Applicant uses the delta doped layer for a different purpose does not alter the conclusion that its use in a prior art device would be prima facie obvious from the purpose disclosed in the reference." In re Lintner, 173 USPQ 560. In this case, even though the purpose of the delta doped layer may be different from that what is stated in the appellant's claims, it does not change the fact that Yamashita also discloses a benefit (i.e. to increase the current drive force of the transistor) of including an n-type delta doped layer that results in a structure that still reads on the appellant's claim. The motivation (i.e. reduces discontinuity of an electric field at an interface between the undoped AlN layer and the undoped GaN layer) does not further limit the claim because the appellant's final structure is still disclosed by Khan in view of Yamashita.

Regarding the appellant's argument on page 5, third paragraph that "an n-type delta doped GaN layer ... having dopant concentration for reducing discontinuity of an electric field at an interface between the undoped AlN layer and the undoped GaN layer" clearly defines the



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structure itself and does not relate to the manner in which the apparatus is intended to be employed, this argument is not persuasive. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F. 2d 1647 (1987). The manner in which the apparatus is intended to be employed does not change the fact that Khan in view of Yamashita still disclose the structural limitations (i.e. an n-type delta doped GaN layer interposed between the undoped AlN layer and the undoped GaN layer) of the appellant's claims, and therefore, still reads on the appellant's claim.

For the sake of arguendo, even if one read the motivation (i.e. for reducing discontinuity of an electric field at an interface between the undoped AlN layer and the undoped GaN layer) into the claim as a patentable limitation, the claim only states that a doping concentration is present in the n-type delta doped GaN layer, and it is ambiguous from the appellant's claim what concentration would achieve this desired motivation. The appellant's claim does not state a relative standard to which this concentration can be determined to achieve this motivation, and therefore, is ambiguous and open to interpretation.

***(11) Related Proceeding(s) Appendix***

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

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For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Eugene Lee/

Primary Examiner, Art Unit 2815

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